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Claims

[c1] 1. A method of testing an integrated circuit (IC) containing a transmit path and a receive path, said method comprising:
connecting said transmit path of said IC to a receive path of a calibrated IC, and said receive path of said IC to a transmit path of said calibrated IC, wherein said IC is provided in the form of a stand-alone die;
transmitting a first signal from said IC to said calibrated IC on said transmit path of said IC;
receiving said first signal in said calibrated IC; and
examining said first signal in said calibrated IC to determine whether to discard/qualify said IC,
wherein the cost to test said IC is minimized due to testing in the form of said die.

[c2] 2.method of claim 1, wherein said IC comprises a mixed signal IC and said calibrated IC is also of mixed signal form, said method further comprising:
converting a first digital data element to an analog signal, wherein said first signal comprises said analog signal, and wherein said analog signal is transmitted on said transmit path of said IC.

[c3] 3. The method of claim 2, wherein said mixed signal IC is connected to said calibrated IC by a probe pad, wherein said probe pad connects a signal lead of said transmit path of said mixed signal IC to a signal lead of said receive path of said calibrated signal IC.

[c4] 4.method of claim 2, further comprising:
converting another digital data element to another analog signal;
transmitting said another analog signal from said calibrated IC to said mixed signal IC; and
examining said another analog signal in said mixed signal IC to determine whether to discard/qualify said mixed signal IC.

[c5] 5. A method of testing a mixed signal integrated circuit (IC), said method comprising:
converting a digital data element to an analog signal in said mixed signal IC;
transmitting said analog signal to said calibrated IC;
receiving said analog signal in said calibrated IC; and
examining said analog signal in said calibrated IC to measure a deviation of a signal level of said analog signal from a signal level corresponding to said digital data element,
wherein a decision to discard/qualify said mixed signal

IC is based on said deviation.

[c6] 6. The method of claim 5, wherein said mixed signal IC is tested in the form of a stand-alone die, wherein a probe pad connects a transmit path of said mixed signal IC to a receive path of said calibrated IC, and a receive path of said mixed signal IC to a transmit path of said calibrated IC.

[c7] 7. The method of claim 5, wherein said mixed signal IC is designed to operate with a plurality of valid symbols contained in a constellation table, wherein each of said plurality of valid symbols contains a plurality of vector components, said method further comprising:
generating in said mixed signal IC each of a plurality of baseband signals by converting a corresponding sequence of vector components, wherein said sequence of vector components comprise said digital data element, wherein corresponding vector components form a transmitted symbol;
modulating each of said plurality of baseband signals with a corresponding one of a plurality of carrier signals to generate a corresponding one of a plurality of modulated signals, wherein each of said plurality of baseband signals are phase-shifted at least by some degree with respect to each other; and
combining in said mixed signal IC said plurality of mod-

ulated signals to generate said analog signal transmitted to said calibrated IC.

[c8] 8. The method of claim 7, further comprising:
demodulating in said calibrated IC, said analog signal using a corresponding one of said carrier signals to generate a corresponding one of a plurality of demodulated signals;
converting each of said plurality of demodulated signals into a corresponding sequence of vector components, wherein corresponding vector components form a vector combination;
determining said deviation based on each of said vector combinations and a corresponding valid symbol.

[c9] 9. The method of claim 8, wherein said determining comprises:
receiving vector components corresponding to said transmitted symbol, wherein said corresponding valid symbol comprises said transmitted symbol; and
computing said deviation based on a vector distance between said transmitted symbol and said vector combination corresponding to said transmitted symbol.

[c10] 10. The method of claim 8, wherein said determining comprises:
finding a closest valid symbol to said vector combina-

tion, wherein said corresponding valid symbol comprises said closest valid symbol; and

computing said deviation based on a vector distance between said vector combination and said closest valid symbol.

[c11] 11. The method of claim 8, wherein said deviation is determined based on 802.11a wire-less standard.

[c12] 12. The method of claim 8, wherein each of said symbols contain only two vector components.

[c13] 13. A mixed signal integrated circuit (IC) containing a built-in-self-test capability, said mixed signal IC comprising:

a receiver block receiving an analog signal, said analog signal being generated externally by converting a digital data element; and

a computation block examining said analog signal to measure a deviation of a signal level of said analog signal from a signal level corresponding to said digital data element,

wherein a decision to discard/qualify said mixed signal IC is based on said deviation.

[c14] 14. The mixed signal IC of claim 13, wherein said mixed signal IC is designed to operate with a plurality of valid

symbols contained in a constellation table, wherein each of said plurality of valid symbols contains a plurality of vector components, said mixed signal IC further comprising a transmitter block, wherein said transmitter block comprises:

a plurality of digital-to-analog convertors generating each of a plurality of baseband signals by converting a corresponding sequence of vector components, wherein corresponding vector components form a transmitted symbol;

a plurality of up-conversion mixers modulating each of said plurality of baseband signals with a corresponding one of a plurality of carrier signals to generate a corresponding one of a plurality of modulated signals, wherein each of said plurality of baseband signals are phase-shifted at least by some degree with respect to each other; and

an adder combining said plurality of modulated signals to generate another analog signal.

[c15] 15. The mixed signal IC of claim 13, wherein said receiver block comprises:

a plurality of down-conversion mixers demodulating said analog signal using a corresponding one of a carrier signals to generate a corresponding one of a plurality of demodulated signals;

a plurality of analog-to-digital convertors converting each of said plurality of demodulated signals into a corresponding sequence of vector components, wherein corresponding vector components form a vector combination;

said computation block comprising a error vector magnitude (EVM) computation block, said EVM computation block determining said deviation based on each of said vector combinations and a corresponding valid symbol.

[c16] 16. The mixed signal IC of claim 15, wherein said EVM computation block receives vector components corresponding to a transmitted symbol based on which said analog signal is formed, said EVM computation block computing said deviation based on a vector distance between said transmitted symbol and said vector combination corresponding to said transmitted symbol.

[c17] 17. The mixed signal IC of claim 15, wherein EVM computation block finds a closest valid symbol to said vector combination, wherein said corresponding valid symbol comprises said closest valid symbol, said EVM computation block computing said deviation based on a vector distance between said vector combination and said closest valid symbol.

[c18] 18. The mixed signal IC of claim 15, wherein said devia-

tion is determined based on 802.11a wire-less standard.

[c19] 19. A mixed signal integrated circuit (IC) containing a built-in-self-test capability, said mixed signal IC comprising:
means for receiving an analog signal, said analog signal being generated externally by converting a digital data element; and
means for measuring a deviation of a signal level of said analog signal from a signal level corresponding to said digital data element,
wherein a decision to discard/qualify said mixed signal IC is based on said deviation.

[c20] 20. The apparatus of claim 19, wherein said mixed signal IC is designed to operate with a plurality of valid symbols contained in a constellation table, wherein each of said plurality of valid symbols contains a plurality of vector components, wherein said means for receiving is operable to:
demodulate said analog signal using a corresponding one of a carrier signals to generate a corresponding one of a plurality of demodulated signals; and
convert each of said plurality of demodulated signals into a corresponding sequence of vector components, wherein corresponding vector components form a vector combination,

wherein said means for measuring computes said deviation based on each of said vector combinations and a corresponding valid symbol.

[c21] 21. The mixed signal IC of claim 20, wherein said means for measuring receives vector components corresponding to a transmitted symbol based on which said analog signal is formed, said means for measuring computing said deviation based on a vector distance between said transmitted symbol and said vector combination corresponding to said transmitted symbol.

[c22] 22. The mixed signal IC of claim 20, wherein means for measuring finds a closest valid symbol to said vector combination, wherein said corresponding valid symbol comprises said closest valid symbol, said means for measuring computing said deviation based on a vector distance between said vector combination and said closest valid symbol.

[c23] 23. A device comprising:
a processing block; and
a mixed signal integrated circuit (IC) containing a built-in-self-test capability, said mixed signal IC comprising:
a receiver block receiving an analog signal, said analog signal being generated externally by converting a digital data element; and

a computation block examining said analog signal to measure a deviation of a signal level of said analog signal from a signal level corresponding to said digital data element,

wherein a decision to discard/qualify said mixed signal IC is based on said deviation.

[c24] 24. The device of claim 23, wherein said mixed signal IC is designed to operate with a plurality of valid symbols contained in a constellation table, wherein each of said plurality of valid symbols contains a plurality of vector components, said mixed signal IC further comprising a transmitter block, wherein said transmitter block comprises:

a plurality of digital-to-analog convertors generating each of a plurality of baseband signals by converting a corresponding sequence of vector components, wherein corresponding vector components form a transmitted symbol;

a plurality of up-conversion mixers modulating each of said plurality of baseband signals with a corresponding one of a plurality of carrier signals to generate a corresponding one of a plurality of modulated signals,

wherein each of said plurality of baseband signals are phase-shifted at least by some degree with respect to each other; and

an adder combining said plurality of modulated signals to generate another analog signal.

[c25] 25. The device of claim 23, wherein said receiver block comprises:

a plurality of down-conversion mixers demodulating said analog signal using a corresponding one of a carrier signals to generate a corresponding one of a plurality of demodulated signals; and

a plurality of analog-to-digital convertors converting each of said plurality of demodulated signals into a corresponding sequence of vector components, wherein corresponding vector components form a vector combination,

said computation block comprising a error vector magnitude (EVM) computation block, said EVM computation block determining said deviation based on each of said vector combinations and a corresponding valid symbol.

[c26] 26. The device of claim 25, wherein said EVM computation block receives vector components corresponding to a transmitted symbol based on which said analog signal is formed, said EVM computation block computing said deviation based on a vector distance between said transmitted symbol and said vector combination corresponding to said transmitted symbol.

[c27] 27. The device of claim 25, wherein EVM computation block finds a closest valid symbol to said vector combination, wherein said corresponding valid symbol comprises said closest valid symbol, said EVM computation block computing said deviation based on a vector distance between said vector combination and said closest valid symbol.